IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Marc Tremblay and William N. Joy		
Title:	IMPLICITLY DERIVED REGISTER SPECIFIERS IN A PROCESSOR		
Application No.:	09/204,479	Filed:	December 3, 1998
Examiner:	David Y. Eng	Group Art Unit:	2155
Atty. Docket No.:	004-3289		

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REPLY BRIEF (37 C.F.R. § 1.193)

This Reply Brief is in response to Examiner's Answer, dated March 8, 2004, having a period for reply set to expire May 10, 2004 (May 8th being a Saturday). This Reply Brief is being submitted in triplicate and fees are provided in the accompanying transmittal.

Attention of the Board is respectfully directed as follows:

(1) Prior Art of Record

In persisting in the appealed from rejection, the Office relies upon the following reference:

Andrew S. Tanenbaum, *Structured Computer Organization*, Prentice-Hall, 1976.

In particular, the Office relies on Section 3.3.5 ("Indexing") thereof, which at the tail end thereof, states that:

> The need to increment or decrement an index register just before or after it is used is so common that some computers provide special instructions, or addressing modes, or even special index registers, which automatically increment or decrement themselves. Automatic modification of an index register is called **autoindexing**. The PDP-11 can use any of

> its general registers for autoindexing. This topic will be discussed in more detail in Section 3.3.8.

Tanenbaum, p. 85 (emphasis added).

Since the essential nature of the Office's argument is based entirely on the meaning of autoindexing as used in the reference, it is somewhat odd that the Examiner failed to include in the copy supplied by Form PTO 892, Section 3.3.8, of Tanenbaum. Of note, the relied-upon 1976 edition of Tanenbaum is out-of-print and not readily-available. Nonetheless, Applicant has now been able to obtain a copy the omitted section and supplies a copy herewith. As the omitted section was apparently omitted by the Office from the supplied copy of art that is already of record, the previously omitted pages would not appear to constitute an amendment, affidavit or other evidence requiring submission as a separate paper.

Of note, with or without Section 3.3.8, applicant's claims are entirely distinguishable over the relied upon combination of Tanenbaum and Baxter. However, Section 3.3.8 serves to emphasize (1) the consistency of Applicant's positions with the actual content of Tanenbaum and (2) the inconsistency of the Office's positions with respect to Tanenbaum. We now turn to the substance.

(2) Response to Rejection and Examiner's Answer

Applicant is somewhat amazed that prosecution has been so arduous given the clear nature of the distinction between Tanenbaum and Applicant's claimed invention. An important aspect of that distinction can be summarized as follow:

Tanenbaum discloses auto-incrementing register contents as a byproduct of instruction execution so that a subsequently executed instruction may use the incremented contents of the register so-incremented. In contrast, Applicant claims (1) *explicitly* identifying one register operated upon by a particular instruction using an explicitly defined register specifier and (2) *implicitly* identifying at least one other register operated upon *by that same instruction* based on *that explicitly defined register specifier*. Tanenbaum discloses that for consumption by a subsequently-executed instruction, register contents can be modified by execution of a prior instruction.

Applicant's technique concerns specification of the particular registers upon which an instruction operates, wherein one particular register is specified explicitly and at least one other register is specified implicitly based on the explicit specification.

More completely:

- **Tanenbaum**: Tanebaum describes auto-incrementing (or auto-decrementing) ***contents of a register*** as a ***byproduct of executing an instruction that uses the register***. Tanenbaum explains on page 84 a motivating instruction sequence:

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  MOVE A,B
  MOVE A+1,B+1
  ```

  where the requirement to provide an incremented (or decremented) memory address in program code for the second instruction can be avoided by employing an index register whose contents may be explicitly incremented (or decremented) after use (i.e., after execution of an instruction that uses contents of the register) and which is employed in the addressing of data in memory. Better still, Tanenbaum points out (on page 85) that special instructions, addressing modes or index registers may be employing to provide ***auto*** indexing, whereby the incrementing (or decrementing) of register contents is automatic.

  The portion of Tanenbaum disclosure relied upon by the Office would seem to make the foregoing clear. Nonetheless, the office persists in characterizing Tanenbaum as "auto-indexing of registers" or more precisely as applied to Applicant's claims, as "auto-indexing of register [specifier]s." Tanenbaum discloses autoindexing of ***register contents***. The datum incremented in Tanenbaum's example is a memory address (e.g., a pointer) stored in a register. Tanenbaum ***does not*** disclose incrementing a register-specifier or indirectly specifying a register-specifier employed by any instruction.

  Applicant respectfully directs the Honorable Board to Section 3.3.8 of Tanenbaum (see above), which reinforces these points by detailing on page 94

of the already cited reference, autoincrement and autodecrement operation of the PDP-11. That description, particularly Fig. 3-30(b) and the accompanying description make it clear that register contents are the items incremented or decremented.

- **Applicant's Claim(s)**: Applicant's claims are broad, but precise. For example, claim 1 requires:

> a functional unit, coupled to the register file, that executes ***an instruction*** that operates upon plural registers of said register file, including ***at least one register explicitly identified by an explicitly defined register specifier and at least one other register implicitly identified by the explicitly-defined register specifier***.

Independent claim 20 (a method), though of substantially differing scope, is similar in distinction.

The Office's continued reliance on Tanenbaum, a reference whose disclosure is unambiguously directed to auto-increment of ***register contents*** by operation of *one instruction* and for consumption of a *subsequent instruction*, is misguided. As a result the prior art has been accorded inordinate scope, the claims have been interpreted in a way that is overbroad, or both. Details of the § 103 analysis appear in the Appeal Brief.

Applicant's claim(s) refer to an instruction that operates on a register that is explicitly identified by a register specifier and at least one register that is implicitly identified by that same register specifier. Presumably, the Office has simply missed the distinction between register contents and register specifiers. In addition, Applicant's claims recite that the explicitly identified register and the implicitly identified register are operated upon by the same instruction. Presumably, the Office has simply missed the distinction between one instruction and two instructions.

CONCLUSION

Insofar as a legal basis for reversal of the Office's outstanding rejection has been detailed in the preceding Appeal Brief, Applicant has attempted to highlight in this Reply Brief, the technical distinctions and simple misinterpretations made by the Office in its representations to this Honorable Board. Examiner's Answer, particularly the statement that:

> Appellant's invention is to applied [sic] the same auto-indexing technique of instruction to operands [sic]. This is exactly Tanenbaum's teaching.

Examiner's Answer at 6, suggests that a misinterpretation of the auto-indexing disclosure of Tanenbaum and a simple disregard for Applicant's actual claim language are central to the legal error represented by the still maintained rejection of Applicant's claims.

For at least the foregoing reasons, together with those reasons outlined in the preceding Appeal Brief, Appellants' presently claimed invention would not have been obvious to one of ordinary skill in the art under 35 U.S.C. § 103(a) in view of the cited prior art. Accordingly, this honorable Board is respectfully requested to reverse the rejections of Claims 1, 3-17, 19-21, and 23-24 and to direct the claims of the present application to be issued.

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